Ordering number : ENN*6746

CMOS IC

LC86E6449

8-Bit Single Chip Microcontroller with the UVEPROM

Preliminary

Overview

The LC86E6449 is a CMOS 8-bit single chip microcontroller with UVEPROM for the LC866400 series.
This microcontroller has the function and the pin description of the LC866400 series mask ROM version, and 48K-byte EPROM. The program data is rewritable. It is suitable to develop the program.

Features

(1) Option switching by EPROM data
The option function of the LC866400 series can be specified by the EPROM data.
LC86E6449 can be checked the function of the trial pieces using the mass production board.
(2) Internal one-time EPROM capacity : 49408 bytes
(3) Internal RAM capacity : 1152 bytes
Used EPROM or RAM capacity are equal ROM or RAM capacity of mask ROM version which applies LC86E6449.

Mask ROM version	EPROM capacity	RAM capacity
LC866448	49152 bytes	1152 bytes
LC866444	45056 bytes	1152 bytes
LC866440	40960 bytes	1152 bytes
LC866436	36864 bytes	1152 bytes
LC866432	32768 bytes	768 bytes
LC866428	28672 bytes	768 bytes
LC866424	24576 bytes	768 bytes
LC866420	20480 bytes	640 bytes
LC866416	16384 bytes	640 bytes
LC866412	12288 bytes	512 bytes
LC866408	8192 bytes	512 bytes

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(4) Operating supply voltage : 4.5V to 6.0V
(5) Instruction cycle time : 1.0μs to 366μs
(6) Operating temperature : +10°C to +40°C
(7) The pin compatible with the LC866400 series mask ROM devices
(8) Applicable mask ROM version : LC866448/LC866444/LC866440/LC866436//LC866432/LC866428 /LC866424/LC866420/LC866416/LC866412/LC866408
(9) Operating temperature : QFC80E (with window)

Notice for use

LC86E6449 is provided for the first release and small shipping of the LC866400 series.
At using, take notice of the followings.

(1) A point of difference LC86E6449 and LC866400 series

Item	LC86E6449	LC866448/44/40/36/32/28/24/20/16/12/08
Operation after reset releasing	The option is specified until 3ms after going to a 'H' level to the reset terminal by dgrees. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to a 'H' level to reset terminal.
Pull-down resistor of the following pins •S0/T0 – S6/T6 •S7/T7 – S15/T15 •S16 – S27 •S28 – S37	Pull-down resistor provided/not provided Not provided Provided (fixed) Provided (fixed) Not provided	Pull-down resistor provided/not provided Specified by the option Provided (fixed) Specified by the option Specified by the option
Operating supply Voltage range (VDD)	4.5V to 6.0V	2.5V to 6.0V
Operating temperature range (Topg)	+10°C to +40°C	-30°C to +70°C
"L" level hold Tr. of the high voltage withstand input terminal	Refer to 'electrical characteristics' on the semiconductor news.	
Power dissipation		

LC86E6449 uses 256 bytes that is addressed on FF00H to FFFFH in the program memory as the option configuration data area. This option configuration cannot execute all options which LC866400 series have. Next tables show the options that correspond and not correspond to LC86E6449.

• A kind of the option corresponding of the LC86E6449

A kind of option	Pins, Circuits	Contents of the option
Input/output form of Input/output ports	Port 0	1. N-channel open drain output 2. CMOS output *1
		1. Pull-up MOS Tr. proveded 2. Pull-up MOS Tr. not provided *2
	Port 1 *1	1. Input : Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output : CMOS
	Port 3 *1	1. Input : No Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output : CMOS
Pull-up MOS Tr. of input ports	Port 7 *1	1. No Pull-up MOS Tr. 2. Pull-up MOS Tr.

*1) Specified in a bit

*2) Specified in nibble unit. The port of N-channel open drain output does not have the Pull-up MOS Tr..

• A kind of the option not corresponding of the LC86E6449

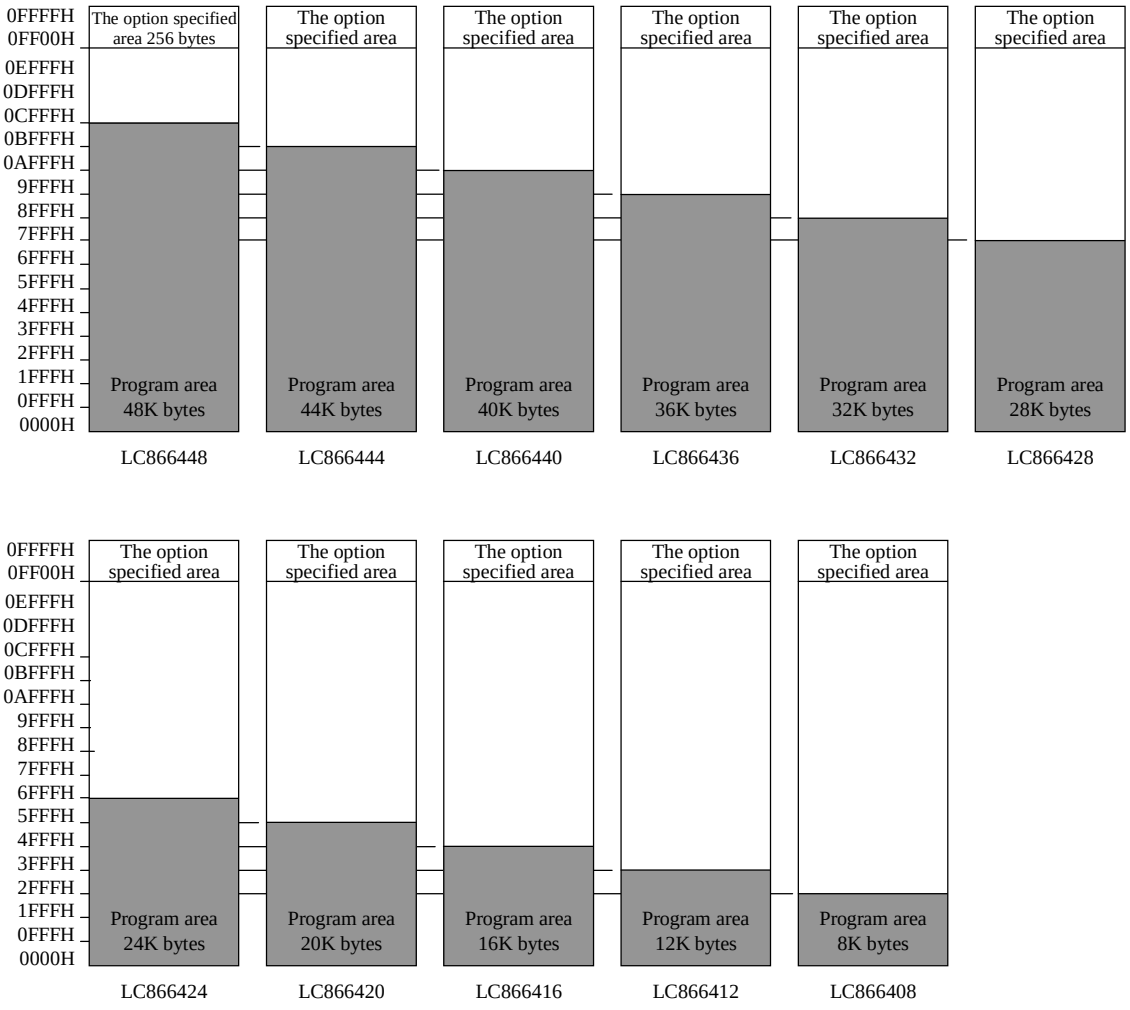
A kind of option	Pins, Circuits	LC86E6449	LC866448/44/40/36/32/28/24/20/16/12/08
Pull-down resistor of	•S0/T0 to S6/T6	Not provided	Specified by the option
the high voltage	•S16 to S27	Provided (fixed)	Specified by the option
Withstand output terminals	•S28 to S37	Not provided	Specified by the option

(2) Option

The option data is created by the option specified program “SU86K.EXE”. The created option data is linked to the program area by linkage loader “L86K.EXE”.

(3) ROM space

LC86E6449 and LC866400 series use 256 bytes that is addressed on 0FF00H to 0FFFFH in the program memory as the option specified data area. These program memory capacity are 61440 bytes that is addressed on 0000H to BFFFH.



How to use

(1) Specification of option

Programming data for EPROM of the LC86E6449 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program, EVA2HEX.EXE. The HEX file is used as the programming data for the LC86E6449.

(2) How to program for the EPROM

LC86E6449 can be programmed by the EPROM programmer with attachment ; W86EP6448Q.

• Recommended EPROM programmer

Productor	EEPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL 1890A

• "27512 (Vpp=12.5V) Intel high speed programming" mode available. The address must be set to "0 to 0FFFFH" and a jumper (DASEC) must be set to 'OFF' at programming.

(3) How to use the data security function

"Data security" is the disabled function to read the data of the EPROM.

The following is the process in order to execute the data security.

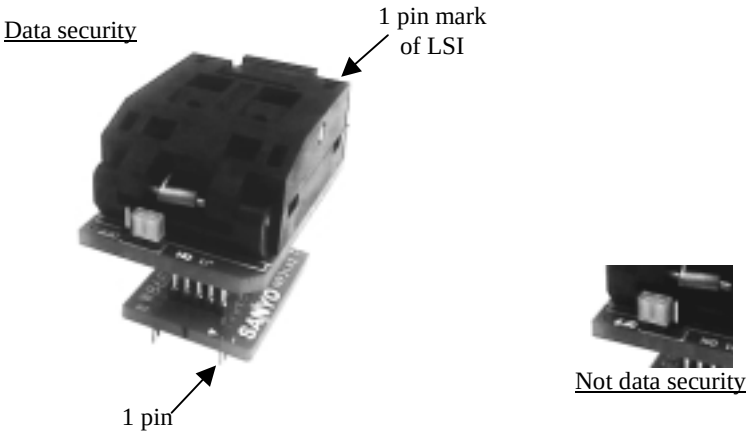
1. Set 'ON' the jumper of attachment.
2. Program again. Then EPROM programmer displays the error. The error means normally activity of the data security. It is not a trouble of the EPROM programmer or the LSI.

Notes

• Data security is not executed when the data of all address have 'FFH' at the sequence 2 above.

• The programming by a sequential operation "BLANK⇒PROGRAM⇒VERIFY" cannot be executed data security at the sequence 2 above.

• Set to 'OFF' the jumper after executing the data security.



W86EP6448Q

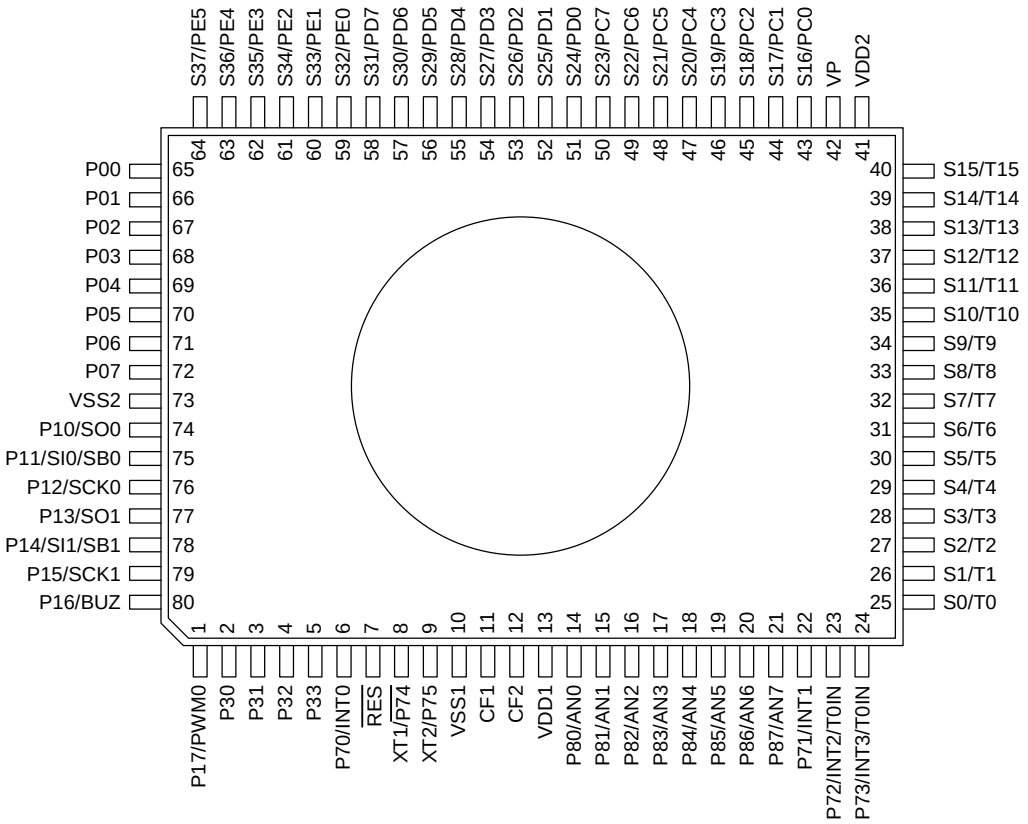
(4) How to eliminate

The programming data can be erased by using the EPROM eraser.

(5) Shielding

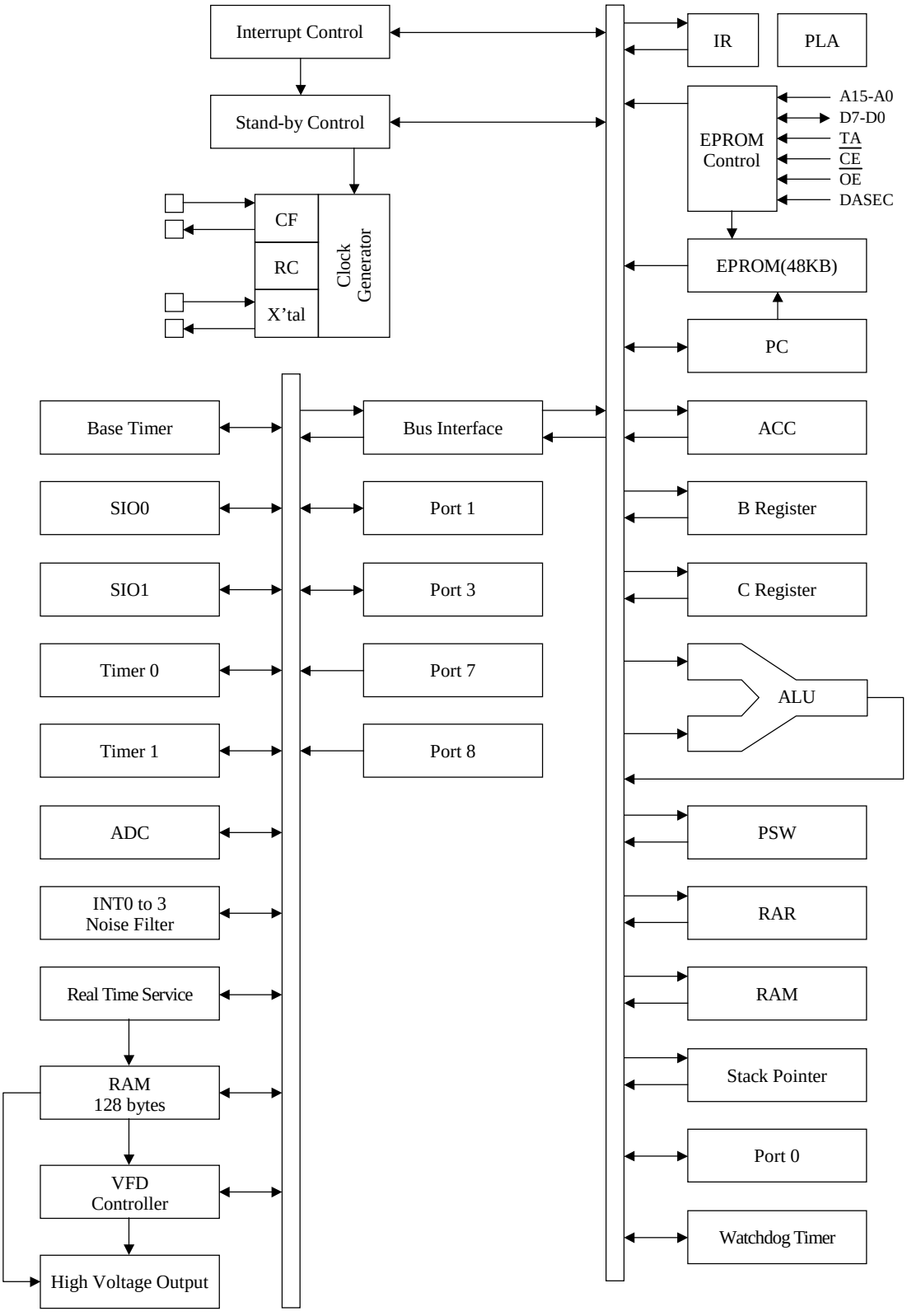
The UVEPROM (ultraviolet erasable programmable ROM) is in it. Put the seal on the window in use.

Pin Assignment



SANYO: QFC80E

System Block Diagram



LC86E6449 Pin description

Pin name	I/O	Function description	Option	EPROM mode
VSS1,2	-	Power pin (-)	-	-
VDD1,2	-	Power pin (+) *4 Refer to Notes	-	-
VP	-	Power pin (-) for the VFD output pull-down resist	-	-
PORT0 P00 to P07	I/O	•8-bit input/output port •Input for port 0 interrupt •Input/output in nibble units •Input for HOLD release •15V withstand at N-channel open drain output	•Pull-up resistor : Provided/Not provided •Output form : CMOS/N-channel open drain	-
PORT1 P10 to P17	I/O	•8-bit input/output port •Input/output can be specified in a bit unit •Other pin functions P10 SIO0 data output P11 SIO0 data input/bus input/output P12 SIO0 clock input/output P13 SIO1 data output P14 SIO1 data input/bus input/output P15 SIO1 clock input/output P16 Buzzer output P17 Timer 1 output (PWM0 output)	•Output form : CMOS/N-channel open drain	Data line D0 to D7
PORT3 P30 to P33	I/O	•4-bit input/output port •Input/output can be specified •15V withstand at N-channel open drain output	•Output form : CMOS/N-channel open drain	-
PORT7 P70 P71 to P75	 I/O I	•6-bit input port •Other functions P70 : INT0 input/HOLD release input/ N-ch Tr. output for watchdog timer P71 : INT1 input/HOLD release input P72 : INT2 input/timer 0 event input P73 : INT3 input with noise rejection filter/timer 0 event input $\overline{P74}$: XT1 terminal for 32.768kHz crystal oscillation P75 : XT2 terminal for 32.768kHz crystal oscillation •Interrupt received forms, the vector addresses	Pull-up resistor : Provided/Not provided (P70,71,72,73) * $\overline{P74}$,P75 don't have pull-up resistor option.	EPROM control signals DASEC (*1) $\overline{OE}$ (*2) $\overline{CE}$ (*3)

	rising	falling	rising & falling	high level	low level	vector
INT0	enable	enable	disable	enable	enable	03H
INT1	enable	enable	disable	enable	enable	0BH
INT2	enable	enable	enable	disable	disable	13H
INT3	enable	enable	enable	disable	disable	1BH

Continue.

Pin name	I/O	Function description	Option	EPROM mode
PORT8 P80 to 87	I	•8-bit input port •Other function AD input port (8 port pins)	-	-
S0/T0 to S6/T6 *6	O	Output for VFD display controller Segment/timing in common	-	-
S7/T7 to S15/T15 *7	O	•Output for VFD display controller Segment/timing with internal pull-down resistor in common	-	TA (*5)
S16 to S31 *8	I/O	•Output for VFD display controller Segment output •Other function S16 : High voltage input port PC0 S17 : High voltage input port PC1 S18 : High voltage input port PC2 S19 : High voltage input port PC3 S20 : High voltage input port PC4 S21 : High voltage input port PC5 S22 : High voltage input port PC6 S23 : High voltage input port PC7 S24 : High voltage input port PD0 S25 : High voltage input port PD1 S26 : High voltage input port PD2 S27 : High voltage input port PD3 S28 : High voltage input port PD4 S29 : High voltage input port PD5 S30 : High voltage input port PD6 S31 : High voltage input port PD7	-	•Address input A15 to A0 •EPROM control signal input
S32 to S37 *9	I/O	•Output for VFD display controller Segment •Other function S32 : High voltage I/O port PE0 S33 : High voltage I/O port PE1 S34 : High voltage I/O port PE2 S35 : High voltage I/O port PE3 S36 : High voltage I/O port PE4 S37 : High voltage I/O port PE5	-	-
$\overline{\text{RES}}$	I	Reset pin	-	-
XT1/$\overline{\text{P74}}$	I	•Input pin for 32.768kHz crystal oscillation •Other function XT1 : Input port $\overline{\text{P74}}$ In case of non use, connect to VDD1.	-	-
XT2/P75	O	•Output pin for 32.768kHz crystal oscillation •Other function XT2 : Input port P75 In case of non use, connect to VDD1 at using as port or unconnect at using as oscillation.	-	-

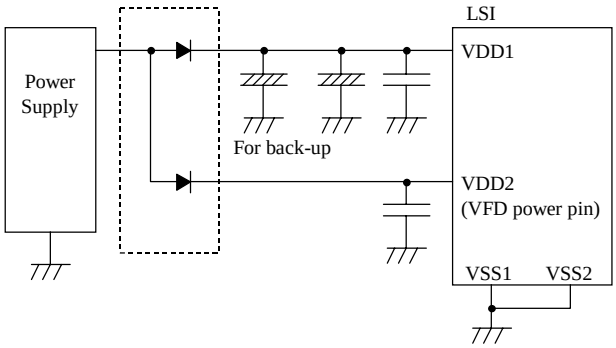
Pin name	I/O	Function description	Option	EPROM mode
CF1	I	Input pin for the ceramic resonator oscillation	-	-
CF2	O	Output pin for the ceramic resonator oscillation	-	-

♦ All of port options except the pull-up resistor option of port 0 can be specified in a bit unit.

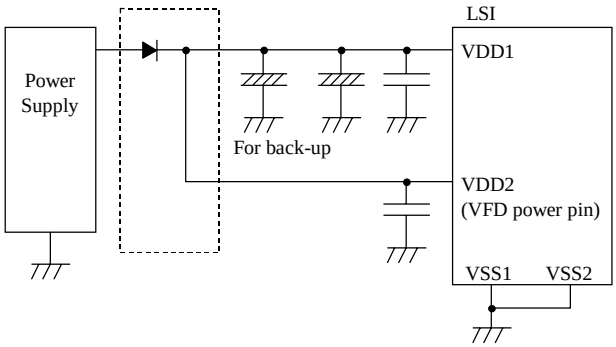
*1 Memory select input for data security
*2 Output enable input
*3 Chip enable input
*4 Connect like the following figure to reduce noise into a VDD1 terminal.
*5 TA → EPROM control signal input
*6 S0/T0 to S6/T6 : not provided the pull-down resistor
*7 S7/T7 to S15/T15 : provided the pull-down resistor (fixed)
*8 S16 to S27 : provided the pull-down resistor (fixed)
*9 S28 to S31 : not provided the pull-down resistor
*10 S32 to S37 : not provided the pull-down resistor

[Notes]
When connecting to the power supply, the power pins must be connected like following figure.

For the LC866448B/44B/40B/36B



For the LC866432A/28A/24A/20A/16A/12A/08A



1. Absolute Maximum Ratings at VSS1=VSS2=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Supply voltage		VDDMAX	VDD1, VDD2	VDD1=VDD2		-0.3		+7.0	V
Input voltage		VI(1)	•Ports 71,72,73, $\overline{74}$,75,8 • $\overline{RES}$			-0.3		VDD+0.3	
		VI(2)	VP			VDD-45		VDD+0.3	
Output voltage		VO(1)	S0/T0 to S15/T15			VDD-45		VDD+0.3	
Input/Output voltage		VIO(1)	•Port 1 •Port 70 •Ports 0, 3 of CMOS output			-0.3		VDD+0.3	
		VIO(2)	Ports 0, 3 of open drain output			-0.3		15	
		VIO(3)	S16 to S37			VDD-45		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 3	•CMOS output •At each pins		-10			mA
		IOPH(2)	S0/T0 to S15/T15	At each pins		-30			
		IOPH(3)	S16 to S37	At each pins		-15			
	Total output current	ΣIOAH(1)	Ports 0,1,3	The total of all pins		-30			
		ΣIOAH(2)	S0/T0 to S15/T15	The total of all pins		-55			
		ΣIOAH(3)	S16 to S37	The total of all pins		-115			
Low level output current	Peak output current	IOPL(1)	Ports 0,1,3	At each pins				20	
		IOPL(2)	Port 70	At each pins				15	
	Total output current	ΣIOAL(1)	Port 0	The total of all pins				40	
		ΣIOAL(2)	Ports 1,3	The total of all pins				40	
Maximum power dissipation		Pdmax	QFC80E	Ta=+10 to+40°C				480	mW
Operating temperature range		Topr				+10		+40	°C
Storage temperature range		Tstg				-55		+125	

2. Recommended Operating Range at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Operating Supply voltage	VDD(1)	VDD1=VDD2	98μs≤tCYC tCYC≤400μs		4.5		6.0	V
Hold voltage	VHD	VDD1=VDD2	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
Pull-down Voltage	VP	VP		4.5 to 6.0	-35		VDD	
Input high voltage	VIH(1)	Port 0 at CMOS output	Output disable	4.5 to 6.0	0.33VDD +1.0		VDD	
	VIH(2)	Port 0 at open drain output	Output disable	4.5 to 6.0	0.75VDD		13.5	
	VIH(3)	•Port 1 •Ports 72,73 •Port 3 at CMOS output	Output disable	4.5 to 6.0	0.75VDD		VDD	
	VIH(4)	Port 3 at open drain output	Output disable	4.5 to 6.0	0.75VDD		13.5	
	VIH(5)	•Port 70 Port input/interrupt •Port 71 • $\overline{RES}$	Output N-channel Tr. OFF	4.5 to 6.0	0.75VDD		VDD	
	VIH(6)	Port 70 Watchdog timer	Output N-channel Tr. OFF	4.5 to 6.0	0.9VDD		VDD	
	VIH(7)	•Port 8 •Ports $\overline{74}$,75	Using as port	4.5 to 6.0	0.75VDD		VDD	
	VIH(8)	S16 to S37	Output P-channel Tr. OFF	4.5 to 6.0	0.33VDD +1.0		VDD	
Input low voltage	VIL(1)	Port 0 at CMOS output option	Output disable	4.5 to 6.0	VSS		0.2VDD	
	VIL(2)	Port 0 at open drain output	Output disable	4.5 to 6.0	VSS		0.25VDD	
	VIL(3)	•Ports 1,3 •Ports 72,73	Output disable	4.5 to 6.0	VSS		0.25VDD	
	VIL(4)	•Port 70 Port input/interrupt •Port 71 • $\overline{RES}$	Output N-channel Tr. OFF	4.5 to 6.0	VSS		0.25VDD	
	VIL(5)	Port 70 Watchdog timer	Output N-channel Tr. OFF	4.5 to 6.0	VSS		0.8VDD -1.0	
	VIL(6)	•Port 8 •Ports $\overline{74}$,75	Using as port	4.5 to 6.0	VSS		0.25VDD	
	VIL(7)	S16 to S37	Output P-channel Tr. OFF	4.5 to 6.0	VP		0.2VDD	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0		6		MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0		3		
	FmRC		RC oscillation	4.5 to 6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	4.5 to 6.0		32.768		kHz

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0				ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0				
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5 to 6.0				s

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Input high current	IIH(1)	Ports 0,3 at open drain output	•Output disable •VIN=13.5V (including off-leakage current of output Tr.)	4.5 to 6.0			5	μA
	IIH(2)	•Ports 1,3 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. •VIN=VDD (including off-leakage current of output Tr.)	4.5 to 6.0			1	
	IIH(3)	•Ports 70,71,72,73 without pull-up MOS Tr. •Port 8	VIN=VDD	4.5 to 6.0			1	
	IIH(4)	$\overline{\text{RES}}$	VIN=VDD	4.5 to 6.0			1	
	IIH(5)	Ports $\overline{74}$,75	Using as port VIN=VDD	4.5 to 6.0			1	
	IIH(6)	S28 to S37	•Output disable •VIN=VDD	4.5 to 6.0			1	
Input low current	IIL(1)	•Ports 1,3 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. •VIN=VSS (including off-leakage current of output Tr.)	4.5 to 6.0	-1			
	IIL(2)	•Ports 70,71,72,73 without pull-up MOS Tr. •Port 8	VIN=VSS	4.5 to 6.0	-1			
	IIL(3)	$\overline{\text{RES}}$	VIN=VSS	4.5 to 6.0	-1			
	IIL(4)	Ports $\overline{74}$,75	Using as port VIN=VSS	4.5 to 6.0	-1			
Output high voltage	VOH(1)	Ports 0,1,3 of CMOS output	IOH=-1.0mA	4.5 to 6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	4.5 to 6.0	VDD-0.5			
	VOH(3)	S0/T0 to S15/T15	IOH=-20mA	4.5 to 6.0	VDD-1.8			
	VOH(4)		•IOH=-1.0mA •The current of these each pins is not over 1mA.	4.5 to 6.0	VDD-1			
	VOH(5)	S16 to S37	IOH=-5mA	4.5 to 6.0	VDD-1.8			
	VOH(6)		•IOH=-1.0mA •The current of these each pins is not over 1mA.	4.5 to 6.0	VDD-1			
Output low voltage	VOL(1)	Ports 0,1,3	IOL=10mA	4.5 to 6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(3)		•IOL=1mA •The current of these each pins is not over 1mA.	4.5 to 6.0			0.4	
	VOL(4)	Port 70	IOL=1mA	4.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	•Ports 0,1,3 •Ports 70,71,72,73	VOH=0.9VDD	4.5 to 6.0	15	40	70	kΩ

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Output off-leakage current	IOFF(1)	•S0/T0 to S6/T6 •S28 to S37 (without pull-down resistor)	•Output P-channel Tr. OFF •VOUT=VSS	4.5 to 6.0	-1			µA
	IOFF(2)		•Output P-channel Tr. OFF •VOUT=VDD-40V	4.5 to 6.0	-30			
'L' level hold Tr. of high voltage withstand input	Rinpd	S16 to S37	Output P-channel Tr. OFF	4.5 to 6.0		400		kΩ
pull-down transistor resistor	Rpd	•S7/T7 to S15/T15 •S16 to S27 (without pull-down resistor)	•Output P-channel Tr. OFF •VOUT=3V •Vp=-30V	5.0	60	100	200	kΩ
Hysteresis voltage	VHIS	•Port 1 •Ports 70,71,72,73 • $\overline{\text{RES}}$	Output disable	4.5 to 6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •VIN=VSS for all unmeasured terminals. •Ta=25°C	4.5 to 6.0		10		pF

4. Serial Input/Output Characteristics at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0,SCK1	Refer to figure 5	4.5 to 6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0,SCK1	•Use pull-up resistor (1kΩ) in the open drain output. •Refer to figure 5	4.5 to 6.0	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set-up time		tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0	0.1			µs
	Data hold time		tCKI				0.1			
Serial output	Output delay time (External clock using for serial transfer clock)		tCKO(1)	•SO0,SO1 •SB0,SB1	•Use pull-up resistor (1kΩ) in the open drain output. •Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0			7/12 tCYC +0.2	
	Output delay time (Internal clock using for serial transfer clock)		tCKO(2)						1/3 tCYC +0.2	

5. Pulse Input Conditions at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	max.	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock selected to 1/1.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock selected to 1/16.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock selected to 1/64.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	128			
	tPIL(5)	$\overline{RES}$	Reset acceptable	4.5 to 6.0	200			µs

6. AD Converter Characteristics at Ta=+10°C to + 40°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	max.	
Resolution	N			4.5 to 6.0		8		bit
Absolute precision (Note 2)	ET			4.5 to 6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC= 0.98µs)		65.28 (tCYC= 4.08µs)	µs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98 µs)		130.56 (tCYC= 4.08µs)	
Analog input voltage range	VAIN	AN0 to AN7		4.5 to 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 6.0			1	µA
	IAINL		VAIN=VSS	4.5 to 6.0	-1			

(Note 2) Absolute precision excepts the quantizing error (±1/2 LSB).
(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current dissipation during basic operation (Note 4)	IDDOP(1)		•FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided	4.5 to 6.0		14	33	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		6	18	
	IDDOP(3)		•FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5 to 6.0		4	13	
	IDDOP(4)		•FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		3	10	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current dissipation in HALT mode (Note 4)	IDDHALT(1)		•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided	4.5 to 6.0		5	14	mA
	IDDHALT(2)		•HALT mode •FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		2.2	7	
	IDDHALT(3)		•HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5 to 6.0		400	1600	μA
	IDDHALT(4)		•HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		25	100	
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)		HOLD mode	4.5 to 6.0		0.05	30	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main-clock)

Oscillation type	Maker	Oscillator	C1	C2
6MHz ceramic resonator oscillation	Murata			
			on chip	
	Kyocera			
3MHz ceramic resonator oscillation	Murata			
			on chip	
	Kyocera			

* Both C1 and C2 must be use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub-clock)

Oscillation type	Maker	Oscillator	C3	C4	Rd
32.768kHz crystal oscillation					

* Both C3 and C4 must be use J rank (±5%) and CH characteristics.
(Not in need of high precision, use K rank (±10%) and SL characteristics.)

(Notes) • Please place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length since the circuit pattern affects the oscillation frequency.
• If you use other oscillators herein, we provide no guarantee for the characteristics.

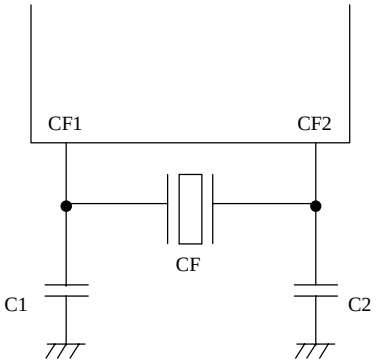


Figure 1 Main-clock circuit
Ceramic resonator oscillation

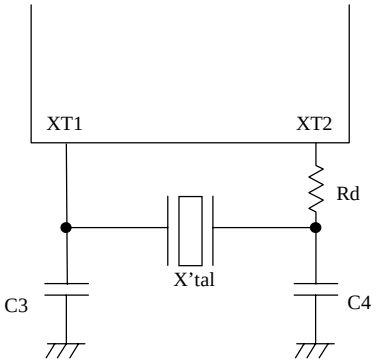


Figure 2 Sub-clock circuit
Crystal oscillation

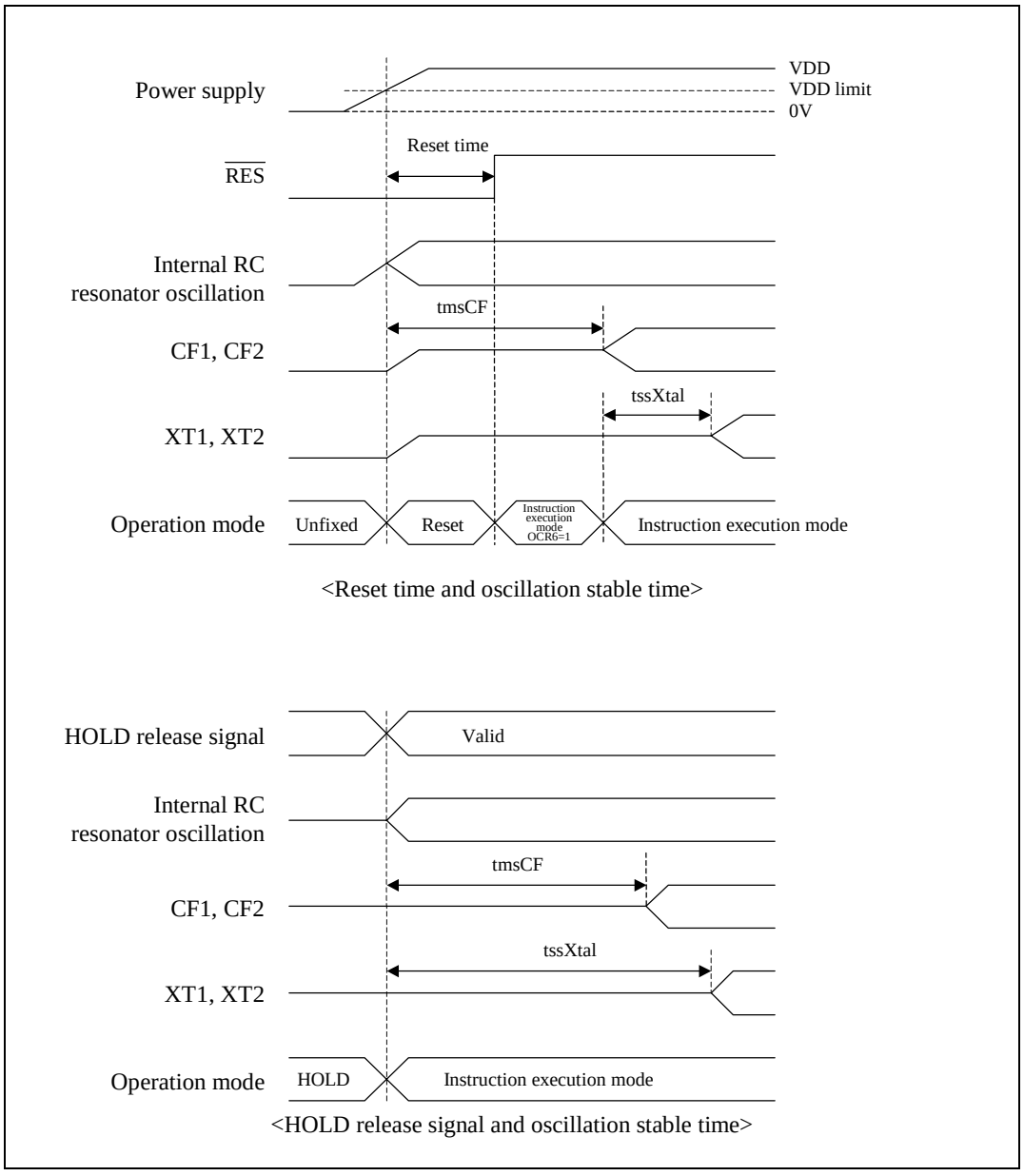
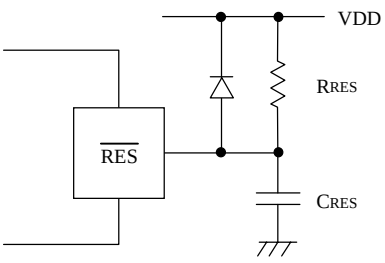


Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

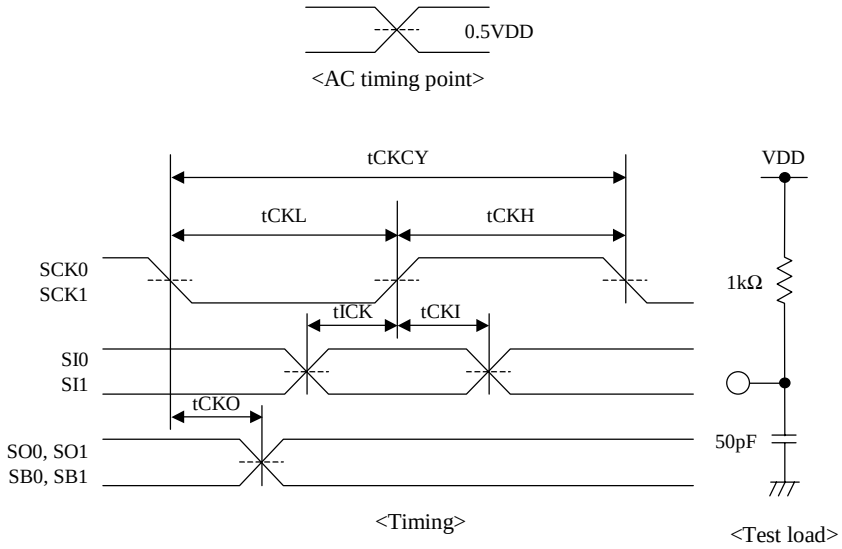


Figure 5 Serial input / output test condition

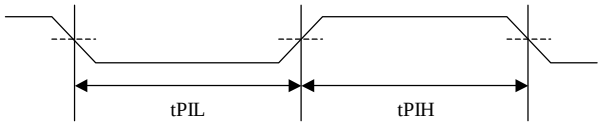


Figure 6 Pulse input timing condition

memo: